

WHAT IS CLAIMED IS:

1 1. A memory system comprising a semiconductor memory for storing
2 digital data, said memory being connectable to a control device for receiving an
3 address signal and making available on a output a data selected by means of an
4 address signal,

5 wherein further comprising a generating circuit for activating of a wait signal to
6 be sent to the control device during reading operations in such a way as to indicate
7 the non availability of the data to be read, and for deactivating the wait signal in such
8 a way as to indicate the availability of the data to be read after a waiting time interval
9 correlated with the actual access time of said memory, this waiting interval having a
10 duration that is variable as a function of the address signal and of at least one
11 operative parameter of said memory system.

1 2. The system according to claim 1, wherein the generating circuit
2 comprises detection means of address transitions such as to receive the address
3 signal as input and generate a detection signal representative of a modification
4 thereof, the generating circuit being such to activate the wait signal starting from the
5 detection signal.

1 3. The system according to claim 2, wherein the address signal carries a
2 plurality of address code groups each referring to a hierarchical domain into which
3 the memory is subdivided, and in which said address transition detection means
4 comprise a plurality of transition detection circuits each intended to generate a
5 corresponding transition signal representative of a modification of one of said code
6 groups, the detection signal being obtained by combining the transition signals.

1 4. The system according to claim 1, wherein the generating circuit
2 comprises circuital means of end-wait signalling for generating an end-wait signal,
3 following said waiting interval, which controls the deactivation of the wait signal.

1 5. The system according to claim 4, wherein said circuital means of
2 signalling comprise at least one dummy circuit block of such a type as to influence
3 the duration of said waiting interval by an amount that is variable as a function of at
4 least one operative parameter of the memory system and according to a behavior

5 essentially reproducing that associated with at least one architectural and/or
6 structural block of the memory system.

1 6. The system according to claim 2, wherein the circuital means of end
2 wait signalling are connected to detection means and comprise a plurality of delay
3 networks each associated with a hierarchical domain of the memory, for receiving a
4 corresponding transition signal as input and to generate a corresponding delayed
5 signal, the end wait signal being obtained by a combination of the delayed signals.

1 7. The system according to claim 6, wherein said plurality of delay
2 networks comprises a first delay network associated with a first hierarchical domain
3 of the memory including a plurality of sub-matrices of the memory, the first delay
4 network being such to introduce into the propagation of the corresponding transition
5 signal which crosses it, a first time delay evaluated on the basis of the actual access
6 time of the memory which occurs following a change in the address signal which
7 implies a change in the sub-matrix within the first hierarchical domain.

1 8. The system according to claim 7, wherein each delay network of the
2 plurality of delay networks comprises a group of dummy circuit blocks each
3 associated with a corresponding architectural block of the memory system or
4 structural block of the memory system, each dummy circuit block introducing a
5 second time delay substantially reproducing that introduced by the architectural or
6 structural block to which it is associated.

1 9. The system according to claim 8, wherein the second time delay of
2 each dummy circuit block is variable as a function of said at least one operative
3 parameter of the memory system and according to a behaviour essentially
4 reproducing that of the corresponding architectural or structural block.

1 10. The system according to claim 1, wherein said at least one operative
2 parameter comprises a memory supply voltage.

1 11. The system according to claim 1, wherein said at least one operative
2 parameter comprises the temperature at which the memory system operates.

1 12. The system according to claim 5, wherein said at least one architectural
2 block is one of the following blocks: an address signal pre-coder, a row decoder, a
3 column decoder, a sense circuit.

1 13. The system according to claim 5, wherein said at least one structural
2 block is one of the following blocks: a memory row, a memory column, a memory
3 cell.

1 14. The system according to claim 1, comprising a device for generating a
2 control device timing signal and in which the generating circuit is such to activate and
3 deactivate the wait signal in an asynchronous manner with respect to the timing
4 signal.

1 15. The system according to claim 1, wherein said memory comprises a
2 flash memory.

1 16. The system according to claim 1, wherein said memory is arranged
2 according to a plurality of hierarchical domains of the type including memory sectors,
3 rows, columns and words.

1 17. The system according to claim 8, wherein at least one of said dummy
2 circuit blocks includes one or more electronic components belonging to the structural
3 block or the architectural block to which the dummy circuit block is associated.

1 18. A wait circuit for a memory having first and second domains
2 respectively having first and second delay times, the wait circuit, comprising:
3 an address-transition-detect circuit operable to receive an address signal
4 having first and second sections that respectively correspond to the first and second
5 domains, to detect a first signal transition in the first section and a second signal
6 transition in the second section, and to generate a first transition-detect signal in
7 response to the first signal transition and a second transition-detect signal in
8 response to the second signal transition; and

9 a delay circuit coupled to the address-transition-detect circuit and operable to
10 transition a wait signal to a wait value in response to the generation of the first or
11 second transition-detect signals and to transition the wait signal to a proceed value,

12 the first delay time after detection of the first signal transition if no tnsition a
13 first delay signal to a proceed value the first delay time after the generation of the
14 first transition-detect signal, to transition a second delay signal to a proceed value
15 the second delay time after the generation of the second transition-detect signal, and

16 to transition the wait signal to a proceed value in response to both of the first and
17 second delay signals having respective proceed values.

1 19. A method, comprising:

2 accessing a memory by transitioning a bit in a section of an address signal,
3 the section corresponding to a domain of the memory having multiple domains, the
4 domain having an access delay; and

5 preventing subsequent access to the memory for or approximately for the
6 access delay.

1 20. A method, comprising:

2 accessing a memory by transitioning bits in first and second sections of an
3 address signal, the first and second sections respectively corresponding to first and
4 second domains of the memory, the first and second domains having respective first
5 and second access delays; and

6 preventing subsequent access to the memory for or approximately for the
7 longer of the first and second access delays.